RF Input Interfaces for ADCs for Next-generation Wireline Communications

You will design input interfaces for ultra high-speed analog-to-digital converters for future internet connections

Popular cloud-based applications such as video-on-demand, internet search engines, streaming, and social media rely all on warehouse-scale data centers, which comprise tens of thousands of computing nodes interconnected via high-capacity optical links, from server-to-server connections up till extended ranges within metro and regional networks. Optical transceivers for these links currently feature data rates in the 100Gb/s to 400Gb/s range, which are achieved by parallelizing several lanes, e.g. 4 lanes of PAM-4-modulated data at >50Gbaud (100Gb/s) per lane. Emerging standards like IEEE 802.3dj and OIF CEI-224G target transmission speeds for 800Gb/s and even 1.6Tb/s with increased lane data rates of 100Gbaud and beyond.

A critical component in state-of-the-art optical transceivers is an analog-to-digital converter (ADC) with moderate resolution and very high sampling rate (>>100GS/s). Such ADC allows the implementation of advanced digital signaling processing (DSP) algorithms for equalization, detection and error correction, which are required to recover the transmitted data from signals that are heavily distorted due to various impairments, including limited bandwidth of front-end electronics, optical modulators and detectors; chromatic dispersion in the optical channel, etc. The ADCs in these systems typically require bandwidths of more than the lane baud rate, resulting in bandwidth specifications of >>100GHz.

CMOS scaling in deep-nanoscale nodes has enabled designing ADCs with very high sampling rates by interleaving several lower-speed channels. However, the sampled signal often suffers from attenuation due to loss over the input buffer, bandwidth limitations and parasitics, for example in a bottom-plate sampling approach. As a result, to achieve the required ENOB level, sampling noise should be lowered sufficiently which poses a limit on the bandwidth that can be achieved for the ADC.

Amplifying the signals instead of just buffering them with signal loss could improve the trade-off but it becomes challenging due to the >>100GHz bandwidth specifications. Besides realizing amplification over a signal bandwidth of >>100GHz, the input interface of such high-speed ADC ideally partially compensates the bandwidth limitations of the sampling network of the ADC while providing sufficiently ESD protection and a sufficiently low return loss. Currently available solutions in CMOS for such ADC input interfaces don't achieve sufficiently high bandwidths, amplification and reliability. This challenge calls for fundamental research into new topologies and implementations for next-generation high-speed interconnections.

The goal of this PhD is to investigate and implement routes for the realization of input interfaces for moderate-resolution ADCs with sampling rates well in excess of 100GS/s. In a first phase, the topology of such amplification, matching and bandwidth-extending network will be defined. The second step of the PhD consists in the actual layout-level implementation of both the critical blocks as well as the whole network for interfacing a very high-speed ADC, in one or more chip tape-outs, which in a final step

will then be characterized using the high-speed measurement infrastructure available at imec.

This PhD takes place in the imec team of Jan Craninckx and Piet Wambacq, one of the world-leading groups in the areas of high-performance RF, millimeter-wave, and ADC design, with a strong publication record in the major conferences and journals of the solid-state circuits community. This is a challenging PhD topic, requiring a highly motivated PhD student with strong interest in developing design skills in advanced CMOS nodes.

Required background: analog/RF IC design
Type of work: 10% literature; 70% design, simulation & layout; 20% measurements
Supervisor: Piet Wambacq
Co-supervisor: Jan Craninckx
Daily advisor: Ewout Martens

Please contact Piet Wambacq (Piet.Wambacq@vub.be) for more information